CLAIMS:

1. An electronic circuit (100) comprising:
a plurality of input/output (I/O) nodes (130) for connecting the electronic circuit to a further electronic circuit via interconnects,
a main unit (110) for implementing a normal mode function of the electronic circuit,
and a test unit (120) for testing the interconnects,
the electronic circuit having a normal mode in which the I/O nodes (130) are logically connected to the main unit (110) and a test mode in which the I/O nodes (130) are logically connected to the test unit (120),
characterised in that in the test mode the test unit (120) is operable as a low complexity memory via the I/O nodes (130).

2. An electronic circuit (100) as claimed in Claim 1, wherein the test unit (120) comprises a Read Only Memory (ROM).

3. An electronic circuit (100) as claimed in Claim 1, wherein the test unit (120) comprises a read/write register.

4. An electronic circuit (402) as claimed in Claim 1, wherein the test unit (406) comprises a combinatorial circuit (502) implementing an XNOR function and being connected to the I/O nodes.

5. An electronic circuit (402) as claimed in Claim 4, wherein a first selection (410) of the I/O nodes are arranged to carry respective input signals and a second selection (412) of the I/O nodes are arranged to carry respective output signals and wherein the test unit (406) is arranged according to the following rules:
each output signal results from an XNOR function having at least two input signals,
each output signal is dependent on a unique subset of the input signals,
each input signal contributes to at least one output signal via a particular XNOR function.

6. An electronic circuit (402) as claimed in Claim 1, wherein the test unit (406) comprises a combinatorial circuit (602) implementing an XOR function and connected to the I/O nodes.

7. An electronic circuit (100) as claimed in Claim 1, wherein the main unit (110) is arranged to bring the electronic circuit (100) into the test mode on receipt via a subset of the I/O nodes (130) of a predefined pattern or sequence of patterns.

8. An electronic circuit (100) as claimed in Claim 1, wherein the electronic circuit is provided with a test control node and wherein the electronic circuit is arranged to switch into the test mode on the basis of a signal value on the test control node.

9. An electronic circuit as claimed in Claim 1, wherein the main unit is a Synchronous Dynamic Random Access Memory (SDRAM) and the test mode is activatable by a read action following power up of the electronic circuit.

10. An electronic circuit (100) comprising:
a plurality of input/output (I/O) nodes (130) for connecting the electronic circuit to a further electronic circuit via interconnects,
a main unit (110) for implementing a normal mode function of the electronic circuit,
and a test unit (120) for testing the interconnects,
the electronic circuit having a normal mode in which the I/O nodes (130) are logically connected to the main unit (110) and a test mode in which the I/O nodes (130) are logically connected to the test unit (120),
characterised in that the test unit comprises at least one combinatorial circuit (502) implementing an XNOR function with at least two function inputs and a function output, the function inputs being connected to particular I/O nodes arranged to operate as input nodes of the test circuit and the function output being connected to a particular I/O node arranged to operate as output node of the test circuit.

11. A method of testing interconnects between a first electronic circuit (100) and a second electronic circuit (210), the first electronic circuit (100) comprising a main unit (110) implementing a normal mode function of the first electronic circuit, and a test unit (120) for testing the interconnects, the method comprising the steps of

logically connecting the test unit (120 ) to the interconnects, and

putting test data on the interconnects by the second electronic circuit (210),

characterised in that the putting step comprises operating the first electronic circuit (100) as a low complexity memory by the second electronic circuit.

12. A method as claimed in Claim 11, wherein the test data comprises an address, the method further comprising the step of generating response data on the interconnects by the first electronic circuit (100), the response data being previously stored in the first electronic circuit (100) at the address.

13. A method as claimed in Claim 12, wherein the test data comprises write data and the putting step comprises storing the write data in the first electronic circuit (100), the method further comprising the step of reading back the stored write data by the second electronic circuit.